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Question Paper Code : 20360

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third/Fifth Semester

Computer Science and Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology).

(Regulations 2013)

(Also common to PTCS 6303 Computer Architecture B.E. (Part-Time) Third Semester – Computer Science and Engineering, Electronics and Communication Engineering — Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Consider three processors P1, P2, and P3 executing the same instruction set. They have clock rates of 3 GHz, 2.5 GHz and 4.0 GHz respectively and CPI of 1.5, 1.0 and 2.2 respectively. Which processor has the highest performance expressed in instructions per second?

2. Classify the instructions based on the operations they perform and give one example to each category.

3. Perform X-Y using 2's complement arithmetic for the given two 16-bit binary numbers X = 0000 1011 1110 1111 and Y = 1111 0010 1001 1101.

4. Define sub-word parallelism.

5. Write the two steps that are common to implement any type of instruction.

6. What is an exception? Give one example for MIPS exception.

7. Web server is to be enhanced with a new CPU which is 10 times faster on computation than old CPU. The original CPU spent 40% of its time processing and 60% of its time waiting for I/O. What will be the overall speedup?

8. Classify shared memory multiprocessor based on the memory access latency.

9. Draw the memory hierarchy in a typical computer system.

10. What is meant by memory–mapped I/O?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3 respectively, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2 respectively. Given a program with a dynamic instruction count of 1.0×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? What is the global CPI for each implementation? Find the clock cycles required in both cases. (7)

(ii) Explain the three broad classes of applications of computers. (6)

Or

(b) (i) Assume that the variables f and g are assigned to registers \$s0 and \$s1 respectively. Assume that the base address of the array A is in register \$s2. Assume f is zero initially.

$f = -g - A[4]$

$A[5] = f + 100$;

Translate the above C statements into MIPS code. How many MIPS assembly instructions are needed to perform the C statements and how many different registers are needed to carry out the C statements? (5)

(ii) Define addressing mode in a computer. What are the different MIPS addressing modes? Give one example instruction to each category. (8)

12. (a) (i) Multiply the following signed numbers using Booth algorithm. $A = (-34)_{10} = (1011110)_2$ and $B = (22)_{10} = (0010110)_2$ where B is multiplicand and A is multiplier. (6)

(ii) Draw the block diagram of integer divider and explain the division algorithm. (7)

Or

(b) (i) How IEEE 752 32-bit single precision floating print numbers represented? Example. How are print numbers represented? (3)

(ii) Explain floating point addition algorithm with a neat block diagram? (10)

13. (a) Draw a simple MIPS datapath with the control unit and explain the execution of ALU instructions. (13)

Or

(b) (i) A processor has five individual stages, namely, IF, ID, EX, MEM, and WB and their latencies are 250ps, 350ps, 150ps, 300ps, and 200ps respectively. The frequency of the instructions executed by the processor are as follows ; ALU : 40%, Branch : 25%, load : 20% and store:15% What is the clock cycle time in a pipelined and non-pipelined processor? If you can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? Assuming there are no stalls or hazards, what is the utilization of the data memory? Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit? (6)

(ii) List the hazards in pipelining a processor and give one example for each. (7)

14. (a) (i) List the software and hardware techniques to achieve Instruction Level Parallelism (ILP). (4)

(ii) Discuss the challenges in parallel processing in enhancing computer architecture. (9)

Or

(b) (i) Explain any three types of hardware multithreading. (9)

(ii) Define the classes in Flynn's Taxonomy of computer architectures. Give one example for each class. (4)

15. (a) (i) Discuss the three mapping techniques in memory hierarchy. Explain with examples. (10)

(ii) Define Translation Lookaside Buffer (TLB). What is its use? (3)

Or

(b) Explain mechanisms Direct Memory Access and Interrupt handling. (6 + 7)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Consider web browsing application. Assuming both client and server are involved in the process of web browsing application, where can caches be placed to speed up the process? Design a memory hierarchy for the system. Show the typical size and latency at various levels of the hierarchy. What is the relationship between cache size and its access latency? What are the units of data transfers between hierarchies? What is the relationship between the data location, data size, and transfer latency?

(ii) The following sequence of instructions are executed in the basic 5-stage pipelined processor:

lw $1, 40($6)

add $6, $2, $2

sw $6, 50($1)

Indicate dependences and their type. Assuming there is no forwarding in this pipelined processor, indicate hazards and add NOP instructions to eliminate them.

Or

(b) Compare hardwired and microprogrammed control unit designs in terms of their mechanism of generating control signals with diagram. (15)